IN THE CLAIMS

1 (Currently Amended). A semiconductor assembly, comprising:

a leadframe <u>having a die flag area;</u>

a die coupled to the [leadframe] <u>die flag area</u>;

a plurality of channels formed [in] <u>on</u> a top surface of the [leadframe] <u>die flag area</u> [for promoting adhesion];

a mold compound for encapsulating the semiconductor assembly wherein the mold compound flows into the plurality of channels and bonds with the plurality of channels forming a lock between the mold compound and the [leadframe] <u>die flag area</u> to prevent delamination of the semiconductor assembly;

[a first raised area on the leadframe where the die is coupled;] and

[a plurality of second raised areas] <u>at least one raised wire bonding area</u> on the [leadframe] <u>die flag area having a wire connected thereto</u> [used for wirebonds wherein the plurality of second raised] <u>wherein the at least one raised wire bonding</u> area[s] allow<u>s</u> the mold compound to [get] <u>flow</u> underneath the wire[bonds and capture the wirebonds to increase reliability of the wirebonds].

2 (Cancelled).

3 (Cancelled).

4 (Currently Amended). The semiconductor assembly in accordance with Claim 1 wherein the [at least one] plurality of channels is triangular in shape.

5 (Currently Amended). The semiconductor assembly in accordance with Claim 1 wherein the [at least one] plurality of channels is "U" shaped.

6 (Currently Amended). The semiconductor assembly in accordance with Claim 4 wherein the [at least] plurality of channels is formed by stamping and coining the leadframe.

7 (Currently Amended). The semiconductor assembly in accordance with Claim 5 wherein the [at least] plurality of channels is formed by etching the leadframe.

8 (Currently Amended). A semiconductor package, comprising:

a leadframe having a die flag area; and

at least one channel formed [in] on a [top] die attach surface of the [leadframe] die flag area wherein the at least one channel prevents delamination of the semiconductor package by allowing a mold compound to flow into the at least one channel [and bonds with the at least one channel forming a lock between the mold compound and the leadframe];

wherein the at least one channel is formed on a metal portion on the die attach surface of the die flag area.

9 (Cancelled).

10 (Currently Amended). The [mounting for a] semiconductor package in accordance with Claim 8 further comprising[:

a first raised area on the leadframe forming a die pad; and]

[a plurality of second raised areas] at least one raised bonding area on the [leadframe] die flag area used for wirebonds wherein the [plurality of second raised areas] raised bonding area allows [a] the mold compound to get underneath [the wirebonds] a wire coupled to the raised bonding area [and] to capture the wire[bonds].

11 (Currently Amended). The [mounting for a] semiconductor package in accordance with Claim 8 [further comprising a plurality of channels formed in the top surface of the leadframe] wherein a semiconductor die is coupled to a central region of the die flag area, the at least one channel located peripherally to where the semiconductor die is coupled and the at least one raised bonding area is peripherally located to the at least one channel.

12 (Currently Amended). The [mounting for a] semiconductor package in accordance with Claim 8 wherein the at least one channel is triangular in shape.

13 (Currently Amended). The [mounting for a] semiconductor package in accordance with Claim 8 wherein the at least one channel is "U" shaped.

14 (Currently Amended). A [mounting for a] semiconductor package, comprising:

a leadframe having a die flag area, the die flag area having a die attach surface;

a semiconductor die coupled to the die attached surface;

[means formed on the leadframe for forming a lock between the leadframe and a mold compound which flows into the means;]

means formed on the [leadframe] die attach surface adjacent to the semiconductor die for forming a lock between [on] the [leadframe] die flag area and a mold compound which flows into the locking means; and

means for wirebonding to a raised portion of the die attach surface [allowing a mold compound to get underneath wirebonds on the leadframe and capture the wirebonds].

15 (Cancelled).

16 (Cancelled).

17 (Cancelled).

18 (Cancelled).

19 (Cancelled).

20 (Cancelled).

21 (Cancelled).

22 (Cancelled).

23 (Cancelled).

24 (Currently Amended). A semiconductor assembly, comprising:

a leadframe having a die pad;

a die coupled to the [leadframe] die pad;

a mold compound for encapsulating the semiconductor assembly; and

means formed [in] on a top surface of the [leadframe] die pad for forming a lock between the mold compound and the [leadframe] die pad;

wherein the means prevents delamination of the mold compound from the die pad.

25 (No Change). A semiconductor assembly in accordance with Claim 24 wherein said means formed [in] on the top surface of the leadframe further is used for allowing the mold compound to flow into the means and bond with the means.

26 (Currently Amended). The semiconductor assembly in accordance with Claim 24 further comprising[:

a first raised area on the leadframe where the die is coupled; and]

at least one raised area [a plurality of second raised areas] on the [leadframe] die pad used for wirebonds wherein the [plurality of second raised areas] at least one raised area allows the mold compound to [get underneath the wirebonds and capture] surround the wirebonds.

27 (No Change). The semiconductor assembly in accordance with Claim 24 wherein the means is formed by stamping and coining the leadframe.

28 (No Change). The semiconductor assembly in accordance with Claim 24 wherein the means is formed by etching the leadframe.

New Claim 29. A semiconductor package in accordance with Claim 14 wherein the semiconductor die is coupled to a central region of the die attached surface and the locking means are located peripherally to the semiconductor die.

New Claim 30. A semiconductor package in accordance with Claim 14 wherein the wirebonding means are located peripherally to the locking means.

New Claim 31. A semiconductor package in accordance with Claim 14 wherein the wirebonding means are located peripherally to the semiconductor die.